New Components for Building Fuzzy Logic Circuits

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Abstract

This paper presents two new designs of fuzzy logic circuit components. Currently due to the lack of fuzzy components, many fuzzy systems cannot be fully implemented in hardware. We propose the designs of a new fuzzy memory cell and a new fuzzy logic gate. Unlike a digital memory cell that can only store either a zero or a one, our fuzzy memory cell can store any value ranging from zero to one. The fuzzy memory cell can also be used as a D-type fuzzy flip-flop, which is the first design of a D-type fuzzy flip-flop. We also designed a new fuzzy NOT gate based only on digital NOT gates that can easily be implemented in CMOS microchips. Our D-type fuzzy flip-flop and fuzzy NOT gate together with fuzzy AND gate and fuzzy OR gate allow us to design and implement fuzzy logic circuits to fully exploit fuzzy paradigms in hardware.

1. Introduction

Currently, fuzzy systems [29, 30, 19, 13, 8, 17] are usually simulated or implemented by using a fuzzifier to convert the inputs, using a set of fuzzy rules for processing and inferring, and using a defuzzifier to convert the results to outputs. To go a step further, researchers are now researching on fuzzy logic circuits that can fully implement fuzzy systems. Fuzzy logic circuits, like digital circuits, can handle all the required functionality in logic gate levels, using fuzzy AND gate, fuzzy OR gate, fuzzy NOT gate, and fuzzy memory cells or flip-flops. However, even these essential fuzzy gates and fuzzy memory cells are not yet fully developed.

We found that fuzzy memory cells or flip-flops reported previously, such as JK-type flip-flop [22, 9, 11] and T-type flip-flop [25], have their limitations and cannot fully be used as general fuzzy memory cells. The flip-flops would not produce the correct results under certain input conditions, as described in the next section.

In this paper, we proposed a new fuzzy memory cell that can also function as a D-type fuzzy flip-flop. Our fuzzy memory cell, unlike a digital memory that can store either a zero or a one, can store any value ranging from zero to one. Furthermore, it is built entirely based on fuzzy logic gates.

We also attempted to realize fuzzy logic gates and memory cells by using CMOS microchip technology, thus that we can easily implement them. Fuzzy OR gate and fuzzy AND gate based on CMOS [27, 3] technology was reported in [5, 2, 1]. However, we need to make small modifications on the reported circuits in order to make them work, as described in Section 4 and 5. Furthermore, we proposed a fuzzy NOT gates that can be implemented using regular NOT gates that can easily be realized in microchip.

The remaining of this paper is organized as follows. Section 2 outlined the related research and their limitations. Section 3 presented our design of a new D-type fuzzy flip-flop, including the simulation results. Section 4 shows a modified fuzzy AND gates. Section 5 shows a modified fuzzy OR gates. Section 6 described our design of a new fuzzy NOT gate, including the implementation and testing results. And, section 7 gave the conclusion and outlined the future research.

2. Related Research

Fuzzy memory cells or fuzzy flip-flops were proposed in [22, 9, 11, 18, 21, 16, 10, 25, 15, 20]. Concept of fuzzy flip flop was first mentioned by Hirota [22]. They used analog gates [14, 26, 7] for the design their JK-type flip-flop as discussed in [28]. Hirota [22] defined fuzzy JK flip-flop based on the binary JK flip-flop but using fuzzy operators. Their design was based on fuzzy operators such as t-norm, s-norm, and fuzzy negation. Consider two fuzzy sets x and y in universe of discourse U, a S-norm operation [4] is defined as,

$$\mu_{x\cup y}(u) = \max[\mu_x(u), \mu_y(u)\}], \quad \forall\ u \in U$$

T-norm operation is defined as

$$\mu_{x\cap y}(u) = \min[\mu_x(u), \mu_y(u)\}], \quad \forall\ u \in U$$

Fuzzy negation is defined as follows:

$$\mu_{\bar{x}}(u) = 1 - \mu_x(u), \quad \forall\ u \in U$$

Based on the fuzzy operations, Hirota [22] defined set-type and reset-type fuzzy flip-flop. Reset-type

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Initial Q	J	K	Q_f 1	2	3
0	4	4	4	2	4
2	4	4	4	2	4
4	4	4	2	4	2
6	4	4	2	4	2

Table 1: One Unstable Condition for the Set-type or Reset-type JK Fuzzy Flip-flop

fuzzy JK flip-flop has the following characteristic equation:

$$Q_R(t+1) = \{J \wedge (1 - Q(t))\} \vee \{(1 - K) \wedge Q(t)\}$$

Characteristic equation for set-type JK fuzzy flip-flop is as follows

$$Q_S(t+1) = \{J \vee Q(t)\} \wedge \{(1 - K) \vee (1 - Q(t))\}$$

However, we can found several unstable conditions for the set-type and the reset-type JK fuzzy flip-flop defined above. Some such examples are provided in Table 1. While the initial stored value of Q is 0v and when given 4v for inputs J and K, the resulting Q will continuously toggling between 4v and 2v. Similar unstable conditions appears when initial stored value is 2 and given 4v for inputs J and K. Other unstable conditions was also observed, but not shown in the table, for values J=K=6, J=4 K=6, and J=6 K=4.

Therefore, neither the set-type nor the reset-type alone can be used as a fuzzy flip-flop. Hirota [22] combined the characteristics of both set-type and reset-type fuzzy JK flip flop and introduced a fundamental equation for fuzzy JK flip flop. The characteristic equation for min-max type fuzzy JK flip flop is as follows:

$$Q(t+1) = \{J \vee \overline{K}\} \wedge \{J \vee Q(t)\} \wedge \{\overline{K} \vee \overline{Q(t)}\}$$

However, above equation also produces unstable conditions such as some shown in Table 1. The authors have tried to eliminate the above unstable conditions by introducing a pair of complicated sample and hold circuits. The sample and hold circuits latch the output during each clock pulse, thus emulating the behavior of a flip-flop. But these circuits are difficult to design and cumbersome to modify. Such circuitry cannot easily be combined with other fuzzy circuitry.

Virant et al. [25] proposed a design of T-type fuzzy flip-flop. The authors have adapted a strategy similar to Hirota [22] in the design of the T fuzzy flip-flop. They introduced the following two equations for T fuzzy flip-flop [25]:

$$Q(t+1) = \max(\min((1-T), Q(t)), \min(T, (1-Q(t))))$$

$$Q(t+1) = \min(\max(T, Q(t)), \max((1-T), (1-Q(t))))$$

However, the T fuzzy flip-flop has its own limitation. For example, it cannot be connected in such a way to produce a D-type fuzzy flip-flop.

$Q(t)$	$D(t)$	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1

Table 2. Excitation Table for Binary D flip-flop.

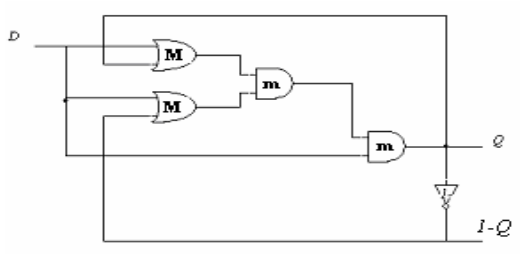


Fig. 1. A New D-type Fuzzy Flip-Flop

Development of fuzzy logic gates, such as fuzzy AND, fuzzy OR, and fuzzy NOT gates, using analog circuit approach were reported in [28, 12, 23, 6]. The design of fuzzy AND gate and fuzzy OR gate using digital CMOS technology was reported [5, 2], in which however, they did not show the design of a fuzzy NOT gate. We tried to implement the results reported in [5. 2] and found that we need to modify the circuits slightly to make them work. We will show the resultant modified circuits in Section 4 and 5.

3. Our Design of a New D-type Fuzzy Flip-flop

In this section we present our design of a new D-type fuzzy flip-flop or fuzzy memory cell. Our design is based on an extension of the idea of binary D flip-flop. Excitation table for binary D flip flop is shown in Table 2.

The next state $Q(t+1)$ of a D fuzzy flip-flop is characterized as a function of both the present state $Q(t)$ and the input state D. Min term expression for $Q(t+1)$ is

$$Q(t+1) = DQ(t) + D\overline{Q(t)}$$

Above equation is also referred to as the characteristic equation of the D Flip-flop. A mutually

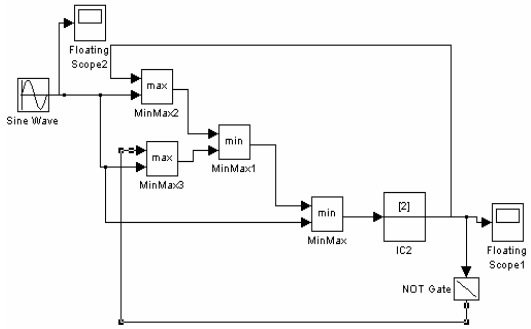
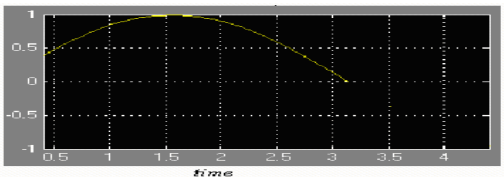
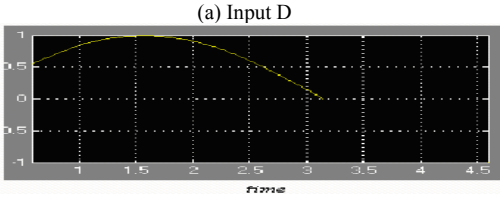


Fig. 2. Simulation Setup of D fuzzy flip-flop using Simulink



(a) Input D



(b) Output Q

Fig. 3. Simulated Result of D fuzzy flip-flop

equivalent equation can be derived from Table 2 consisting of max terms

$$Q(t+1) = \left(D + Q(t)\right) \cdot \left(D + \overline{Q(t)}\right)$$

Above two equations can be transformed to fuzzy domain by replacing the binary operators by fuzzy operators. They can be redefined using min-max type operation and fuzzy negation as follows:

$$Q(t+1) = \{(1 - Q(t)) \wedge D\} \vee \{Q(t) \wedge D\}$$

$$Q(t+1) = \{(1 - Q(t)) \vee D\} \wedge \{Q(t) \vee D\}$$

In which the $\wedge$ represents min operation and $\vee$ represents max operation. These two equations, however, do not completely transform D flip-flop to the fuzzy domain. Hence, we proposed an equation that has the characteristics of both the equations and also exhibits an analogy with the binary counterpart, as follows:

$$Q(t+1) = \{D\} \wedge \{D \vee Q(t)\} \wedge \{(1 - Q(t)) \vee D\}$$

This equation has led to realization of the circuit of D fuzzy flip-flop. The design of the new D fuzzy flip-flop is shown in Fig. 1. This D fuzzy flip-flop can be used as a fuzzy memory cell.

Working of the D fuzzy flip-flop (shown in Fig. 1) can be understood by initially considering binary values 0 or 1. If the value of the input D is set at either 0 or 1 regardless the initial value of Q at time t, Q will be set to the value of D. Any value ranging from 0 to 1 also produce the required results. To get an initial idea of the behavior of the D fuzzy flip-flop, we simulated our design using MATLAB and Simulink [24]. Fig. 2

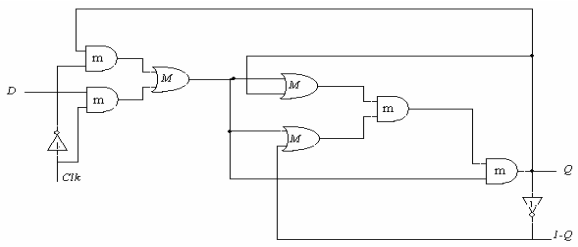


Fig. 4. Clocked D Fuzzy Flip Flop

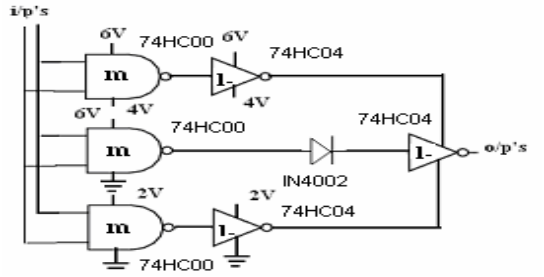


Fig. 5. Modified Fuzzy AND gate

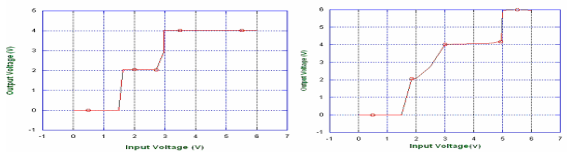
shows the setup of the simulation and the results are shown in Fig. 3. The results show that the D fuzzy flip-flop is simply storing whatever value provided on the input D. It is simply a fuzzy memory cell.

We extended the fuzzy memory cell to clocked D fuzzy flip-flop. Fig. 4 shows our design of the fuzzy flip-flop. This clocked D fuzzy flip-flop can be used in the design of sequential fuzzy circuits.

4. A Modified Fuzzy AND gate

The design of D fuzzy flip-flop described in the last section can be implemented using fuzzy AND gate, fuzzy OR gate, and fuzzy NOT gate. These fuzzy gates can be realized using analog approach as reported in [28, 12, 23]. However, the resulting circuits are difficult to be implemented using current microchip technology. Thus, researchers attempted to use digital approach for the design of the fuzzy gates. The digital approach, however, does not produce the true fuzzy gates, but produces many-valued logic gates. These many-valued logic gates are easier to be implemented using current microchip technology. In this section we will shows a many-valued AND gates while a many-valued OR gates and NOT gates are shows in the subsequent sections.

Fig. 5 shows the circuit of a modified fuzzy AND gate, which is based on the design provided in [5, 2]. When we tried to implement the design reported in [5] using discrete components, such as microchip 74HC04 and 74HC00, we encountered small problem and need to introduce a diode as shown in Fig. 5. The diode blocks reverse current from the output, without which wrong results are produced. This modification may reflect the special needs in the use of discrete components and does not necessary imply any fault in the design.



(a) One input held at 4v (b) One input held at 6v

Fig. 6. Test results of the modified fuzzy AND gate

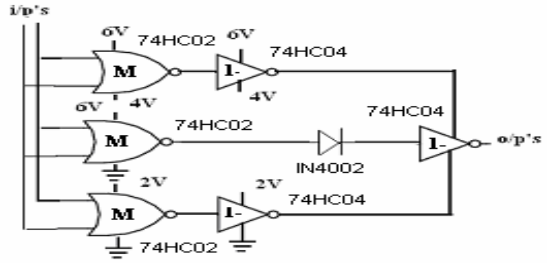


Fig. 7. Modified Fuzzy OR gate

One test result of the modified fuzzy AND gate is shown in Fig. 6. In this test, one of the input to the AND gate is hold at 4v, while the other input allows to vary from 0 to 6v. The output is shown in the figure. Fig. 7 shows another test care where one of the inputs is held at 6v and the other input is allowed to vary from 0 to 6v. These test results does not fully matched the ideal behavior. For example, the ideal case for the output in Fig. 7 should be prefect steps. Nevertheless, these results showed the AND gate behaves like a many-valued logic gate having min function.

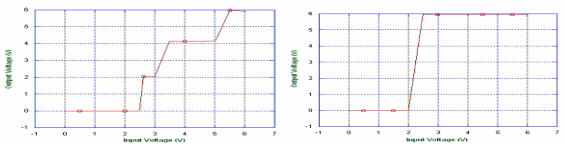
5. A Modified Fuzzy OR gate

Fig. 7 shows the circuit of a modified fuzzy OR gate, which is based on the design provided in [5, 2]. The modification is similar to that of the AND gate by introducing one diode to prevent the reverse current. Fig. 8 show some test results. Fig. 8(a) shows the results of a test care where one input is hold at 2v and the other input is allowed to vary from 0 to 6v. Fig. 8(b) shows the results of another test care where one input is hold at 6v and the other input is allowed to vary from 0 to 6v. Despite some imperfections, the results show the OR gate behaves like many-valued OR gate having max function.

6. Our Design of a New Fuzzy NOT Gate

We attempted to design a fuzzy NOT gate using digital approach, which resulted in a many-valued NOT gate. The design is shown in Fig. 9. This design uses only digital NOT gate as building block. Like the fuzzy AND gate, and fuzzy OR gate case, it required a diode to prevent reverse current.

As shown in the figure, the digital NOT gates are supplied by different value of voltages. We have tried many different combinations and so far the combination


(a) One input held at 2v (b) One input held at 6v
Fig. 8. Test results of the modified OR gate

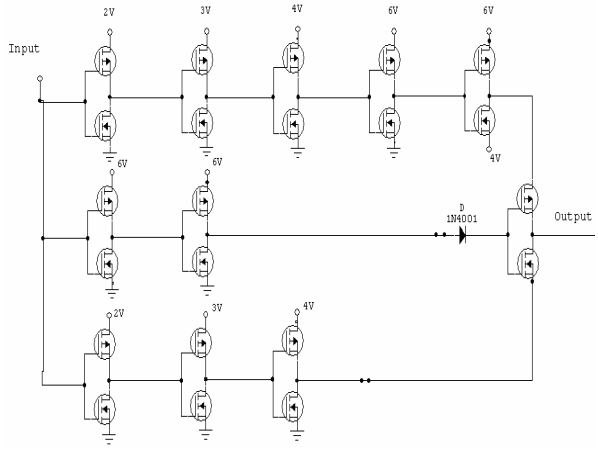


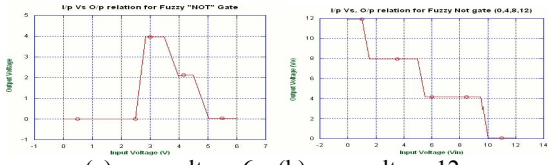
Fig. 9. A Design of fuzzy NOT gate (many-valued version).

of voltage in the figure produced the best result in the case we limited the maximum voltage to be 6v. Fig. 10(a) shows the result of one test. The gate begins to behave like a many-valued NOT gate after the input voltage rising to 2.5v. This is due to the threshold voltage required to switch the transistors. If we allowed the supply voltage to reach max 12v and scaled the supply voltages to each digital NOT gate accordingly, we are able to get better results as shown in Fig. 10 (b). Although this digital approach is easier to be implemented in microchip technology, it requires several supply voltages.

7. Conclusion and Future Research

This paper presented the design of the first D-type fuzzy flip-flop that can also be used a fuzzy memory cell. It also presented the circuit of a clocked D fuzzy flip-flop that can be used in the design of sequential fuzzy circuits. The D fuzzy flip-flop is a truly fuzzy component that allows any logical value arranging from 0 to 1 to be stored.

The fuzzy flip-flop is designed entire in the fuzzy domain using fuzzy AND gate, fuzzy OR gate, and fuzzy NOT gate. Thus, the realization of the flip-flop depends on the realization of the fuzzy logic gates. We then investigated the hardware realization of the fuzzy logic gates. In here, we concentrated on digital approach, which results in many-valued logic gates. We slightly modified existent designs of the many-valued AND gate and OR gate in an attempt to test



(a) max voltage 6v (b) max voltage 12v
Fig. 10. Test results of fuzzy NOT gate

them using discrete components. We then proposed a design of many-valued NOT gate. However, using off-the-shelf discrete components, the test results do not produce ideal outputs.

Thus, future research may focus on the improvement on the realization of many-valued logic gates as well as the improvement on the realization of truly fuzzy logic gates. The next stage for future research will be to use these fuzzy logic gates and fuzzy flip-flop to design large scale sequential fuzzy circuits and to implement fuzzy systems.

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