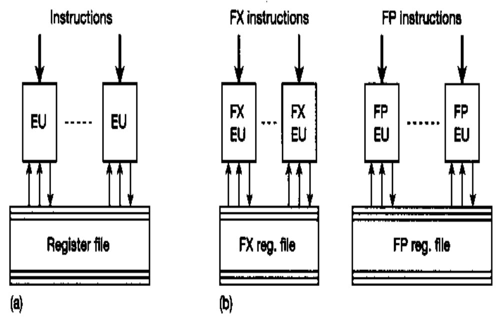
6 VLIW Architectures

- {Very Long Instruction Word}
- {EPIC: Explicit Parallel Instruction-set Computer}
- {**CISC → RISC →EPIC**}
- 6.1 Basic principles
- 6.2 Overview of proposed and commercial VLIW architectures
- 6.3 Case study: The Trace 200 family

TECH
Computer Science

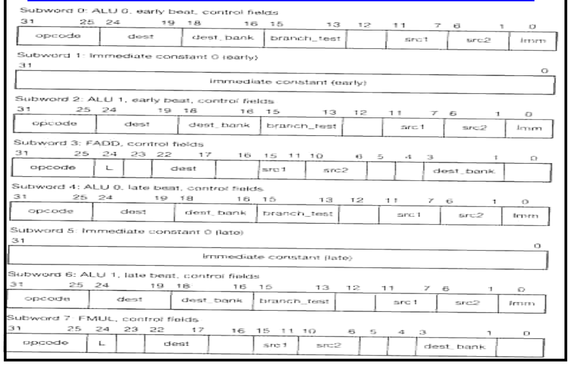
Basic Structure of VLIW Architecture



Basic principle of VLIW

- Controlled by very long instruction words
  - **comprising a control field for each of the execution units**
- Length of instruction depends on
  - **the number of execution units (5-30 EU)**
  - **the code lengths required for controlling each EU (16-32 bits)**
  - **256 to 1024 bits**
- Disadvantages: on average only some of the control fields will actually be used
  - **waste memory space and memory bandwidth**
  - **e.g. Fortran code is 3 times larger for VLIW (Trace processor)**

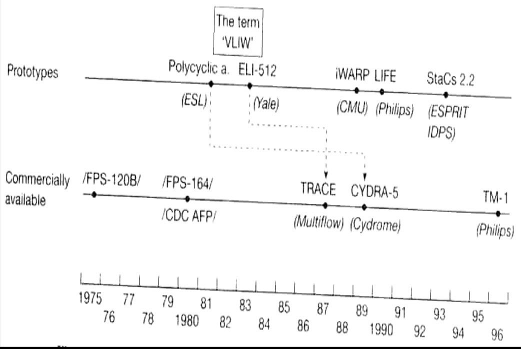
Instruction word format: Trace 7/200


Subword 0: ALU 0, early beat, control fields
31 25 24 19 18 16 15 13 12 11 7 6 1 0
opcode | dest | dest_bank | branch_test | | src1 | src2 | imm
Subword 1: Immediate constant 0 (early)
31 0
immediate constant (early)
Subword 2: ALU 1, early beat, control fields
31 25 24 19 18 16 15 13 12 11 7 6 1 0
opcode | dest | dest_bank | branch_test | | src1 | src2 | imm
Subword 3: FADD, control fields
31 25 24 23 22 17 16 15 11 10 6 5 4 3 1 0
opcode | L | | dest | | src1 | src2 | | | dest_bank |
Subword 4: ALU 0, late beat, control fields
31 25 24 19 18 16 15 13 12 11 7 6 1 0
opcode | dest | dest_bank | branch_test | | src1 | src2 | imm
Subword 5: Immediate constant 0 (late)
31 0
immediate constant (late)
Subword 6: ALU 1, late beat, control fields
31 25 24 19 18 16 15 13 12 11 7 6 1 0
opcode | dest | dest_bank | branch_test | | src1 | src2 | imm
Subword 7: FMUL, control fields
31 25 24 23 22 17 16 15 11 10 6 5 4 3 1 0
opcode | L | | dest | | src1 | src2 | | | dest_bank |

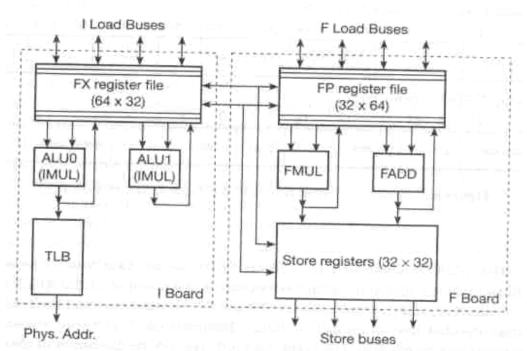
VLIW: Static Scheduling of instructions/

- Instruction scheduling done entirely by [software] compiler
- Lesser Hardware complexity translate to
  - **increase the clock rate**
  - **raise the degree of parallelism (more EU); {Can this be utilized?}**
- Higher Software (compiler) complexity
  - **compiler needs to aware hardware detail**
    - number of EU, their latencies, repetition rates, memory load-use delay, and so on
    - cache misses: compiler has to take into account worst-case delay value
  - **this hardware dependency restricts the use of the same compiler for a family of VLIW processors**

6.2 overview of proposed and commercial VLIW architectures



6.3 Case study: Trace 200



Trace 7/200

- 256-bit VLIW words
- Capable of executing 7 instructions/cycle
  - **4 integer operations**
  - **2 FP**
  - **1 Conditional branch**
- Found that every 5th to 8th operation on average is a conditional branch
- Use sophisticated branching scheme: multi-way branching capability
  - **executing multi-paths**
  - **assign priority code corresponds to its relative order**

Trace 28/200: storing long instructions

- 1024 bit per instruction
- a number of 32-bit fields maybe empty
- Storing scheme to save space
  - **32-bit mask indicating each sub-field is empty or not**
  - **followed by all sub-fields that are not empty**
  - **resulting still 3 time larger memory space required to store Fortran code (vs. VAX object code)**
  - **very complex hardware for cache fill and refill**
- Performance data is Impressive indeed!

Trace: Performance data

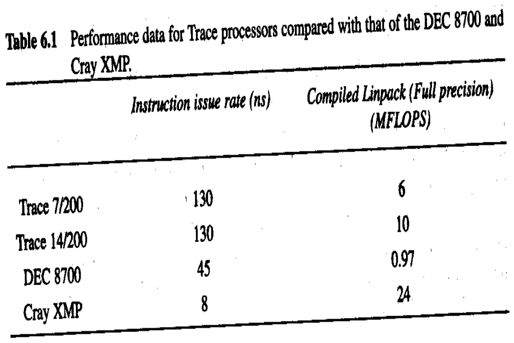
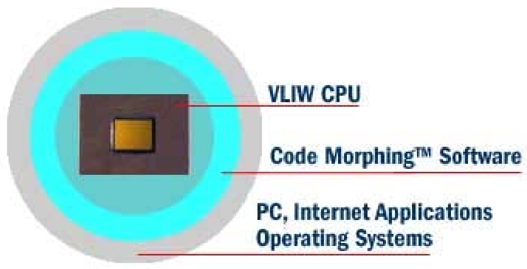


Table 6.1 Performance data for Trace processors compared with that of the DEC 8700 and Cray XMP.

	Instruction issue rate (ns)	*Compiled Linpack (Full precision) (MFLOPS)*
Trace 7/200	130	6
Trace 14/200	130	10
DEC 8700	45	0.97
Cray XMP	8	24

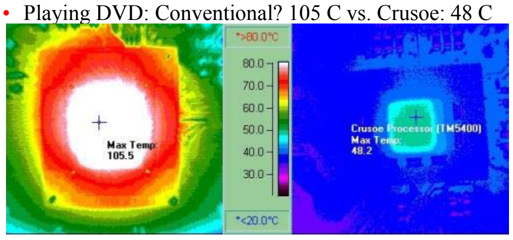
Transmeta: Crusoe

- Full x86-compatible: by dynamic code translation
- High performance: 700MHz in mobile platforms

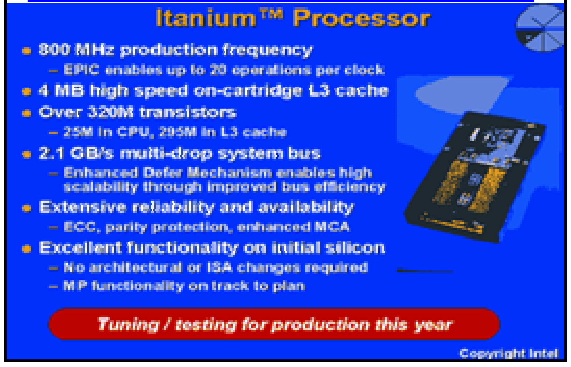


Crusoe

- “Remarkably low power consumption”
  - **“A full day of web browsing on a single battery charge”**
  - **(333-400Mhz TM3120 in production now, running Linux! TM5400 runs Windows, production mid 2000)**
- Playing DVD: Conventional? 105 C vs. Crusoe: 48 C



Intel: Itanium (VLIW) {EPIC} Processor



Itanium™ Processor

- 800 MHz production frequency
  - EPIC enables up to 20 operations per clock
- 4 MB high speed on-cartridge L3 cache
- Over 320M transistors
  - 25M in CPU, 295M in L3 cache
- 2.1 GB/s multi-drop system bus
  - Enhanced Defer Mechanism enables high scalability through improved bus efficiency
- Extensive reliability and availability
  - ECC, parity protection, enhanced MCA
- Excellent functionality on initial silicon
  - No architectural or ISA changes required
  - MP functionality on track to plan

Tuning / testing for production this year

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